

CPRE 4920 Status Report 01

12/18/2025 – 02/04/2026

Group number: SDMay26-24

Project title: Digital ASIC Fabrication

Client &/Advisor: Dr. Henry Duwe

Team Members/Role:

<i>Colin McGann</i>	<i>-Project Lead</i>
<i>Samuel Forde</i>	<i>-PCB & Layout Lead</i>
<i>Michael Drobot</i>	<i>-Firmware Lead</i>
<i>Jack Tonn</i>	<i>-Testbench and Validation Lead</i>
<i>Dawud Benedict</i>	<i>-Cache Lead</i>
<i>Emil Kosic</i>	<i>-Repository and Coding Standards Lead</i>
<i>Joshua Arceo</i>	<i>-Client/Advisor Communications Lead</i>

○ Weekly Summary

Since the end of 4910, we completed major parts of our design in our implementation. This includes implementing the ISA in the cores, the creation of the core controller, connecting the rasterizer to the cores, and verifying the rasterizer on FPGA.

○ Past Week Accomplishments

- Colin McGann: Worked on textures, SPI mem fixes, shaded vertex cache, reorder controller, and FPGA fixes and verification.
- Jack Tonn: Implemented most of the core features and approved many merge requests for the core submodules, along with working on them. Currently we have all the submodules we hopefully will need.
- Dawud Benedict: Created metadata cache HDL. Working on testing SRAM and cache timeliness.
- Michael Drobot: Updated and finalized the ISA and instruction encodings. Finished the core simulator and validated instructions in test_core.s and div/mod procedures

in test_procedures.s. Validated all assembly examples using core simulator. Created the core controller, dispatcher, and index fetcher.

- Sam Forde: Integrated commercial on-chip SRAM into testing SVunit and Caravel frameworks. Worked on getting SRAM hardened as a module. Started rewriting the SPI test model for the external SRAM chip.
- Josh Arceo: Wrote and synthesized accumulator sub module for core. Began writing and testing area optimization script
- Emil Kasic: Implemented and hardened core sub module and worked on refactoring wb to pk bridge and documenting.

○ **Pending Issues**

- Core implementation
- Core controller test
- FPGA Working

○ **Individual contributions**

<u>NAME</u>	<u>Individual Contributions</u>	<u>Hours this period</u>	<u>HOURS cumulative</u>
Colin McGann	Worked on textures, SPI mem fixes, shaded vertex cache, reorder controller, and FPGA fixes and verification.	100	230
Jack Tonn	Core implementation and integration, and submodule approving	99	190
Dawud Benedict	SRAM-Mem Metadata, Cache HDL	32	98
Michael Drobot	ISA finalization, core simulator, core controller, dispatch, index fetcher	80	232
Sam Forde	SRAM testing and module hardening, spi_chip.v investigation	28	87
Josh Arceo	Core accumulator, area optimizer script	40	80
Emil Kasic	Core submodule implementation and testing, Wb to pk refactoring	45	89

○ **Plans for the upcoming weeks**

- Colin McGann: Continue working on getting FPGA to work better.
- Jack Tonn: Core memory read/write, and inbox

- Dawud Benedict: Verification of cache. SVUnit test
- Michael Drobot: Finish verification of core controller/dispatch/index fetcher, get it hardened (waiting on commercial SRAM), and start putting high-level things together.
- Sam Forde: Get SRAM hardened, rewrite spi_chip.v
- Josh Arceo: Polish off area optimizer, use it to create a table of best areas for each module
- Emil Kosic: complete wb to pk with documented signals and state machine diagram